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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,541	01/11/2002	Takehiko Yamakawa	MTS-3300US	9446

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EXAMINER	
LE, LANA N	

ART UNIT	PAPER NUMBER
2685	

DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/044,541	YAMAKAWA ET AL.	
	Examiner	Art Unit	
	Lana N Le	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 02/28/05

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-8, 16-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8, 16-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) 9-15, 25 are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 05/07/02
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 5-6, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Toshihiko et al (JP 09-320,849).

Regarding claim 1, Toshihiko et al disclose a multilayer electronic component having a multilayered product laminating a plurality of dielectric sheets (upper and lower dielectric layers; paragraph 8) as one piece,

a plurality of grounded electrodes (inherent ground electrodes on upper ground layer and lower ground layer) provided among said dielectric sheets (upper and lower dielectric layers; para. 8) being different inside said multilayered product,

inductor electrodes provided on said dielectric sheet surfaces (laminated spiral inductor on upper surface of lower dielectric layer; paragraphs 8-9) not having said plurality of grounded electrodes inside wherein all or part of said inductor electrodes (spiral inductors) are placed (on top of lower dielectric layer) as not to be sandwiched by said plurality of grounded electrodes (spiral inductors show through the upper dielectric

layer due to a portion that is removed or an opening in the upper dielectric layer containing an upper ground layer thereon; para. 9).

Regarding claim 2, Toshihiko et al disclose the multilayer electronic component according to claim 1, wherein the part of said inductor electrodes not sandwiched by said plurality of grounded electrodes is one portion of one inductor electrode (one of spiral inductor on the spiral shaped pattern layer on upper surface of dielectric layer shown through opening of upper dielectric layer; para. 11).

Regarding claim 3, Toshihiko et al disclose the multilayer electronic component according to claim 1, wherein the part of said inductor electrodes not sandwiched

by said plurality of grounded electrodes are one piece or a plurality of pieces of a plurality of the inductor electrodes (spiral inductors on the spiral shaped pattern layer on upper surface of dielectric layer shown through opening of upper dielectric layer; para. 11).

Regarding claim 5, Toshihiko et al disclose the multilayer electronic component according to claim 1 or 2 wherein the part of said inductor electrodes not sandwiched by said plurality of grounded electrodes are placed on the dielectric sheets (upper surface laminated with inductors on the bottom dielectric layer) sandwiched by said plurality of grounded electrodes.

Regarding claim 6, Toshihiko et al disclose the multilayer electronic component according to claim 1 or 2 wherein part of said inductor electrodes not sandwiched by said plurality of grounded electrodes are formed by having slots (openings on upper

face of upper ground layer) formed on said grounded electrodes (upper ground layer) overlap said inductor electrodes (para. 9).

Regarding claim 8, Toshihiko et al disclose the multilayer electronic component according to claim 2 or 3, wherein part and other remaining portions of said inductor electrodes sandwiched by said plurality of grounded electrodes are placed on said dielectric sheets that are the same (all inductors form on upper surface of same lower dielectric layer; paras. 9, 11).

3. Claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toshihiko et al (JP 09-320849) in view of Masao et al (JP 06-20839).

Regarding claim 16, Toshihiko et al disclose the multilayer electronic component according to claim 3, wherein Toshihiko et al do not disclose an inductor comprised of part of said inductor electrodes not to be sandwiched by said plurality of grounded electrodes is used low-pass filter, and the inductor comprised of the inductor electrodes other than said part thereof is used in a band pass filter.

Masao et al disclose wherein an inductor comprised of part of said inductor electrodes (7 on bottom green sheet 1a) not to be sandwiched by said plurality of grounded electrodes is used in a filter, and the inductor (3a on layer 1b) comprised of the inductor electrodes other than said part thereof (part sandwiched between layer 1c and 1a) is used in a filter (paras. 9-10). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the inductor electrodes of

Toshihiko et al in a filter in order to allow the filter to have high inductance as suggested by Masao et al (para. 1).

Toshihiko et al and Masao et al do not disclose the inductor electrodes is used in a low pass filter or a high pass filter. However, it is well known in the art that a filter can be low pass or high pass based on the desired frequency response. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the inductor be used in a low or high pass filter based on which unwanted frequencies the electronic component needs to filter out to optimize conductance.

Regarding claim 17, Toshihiko et al disclose the multilayer electronic component according to claim 3, wherein Toshihiko et al do not disclose an inductor comprised of part of said inductor electrodes not to be sandwiched by said plurality of grounded electrodes is used in a band-pass filter, and the inductor comprised of the inductor electrodes other than said part thereof is used in a high-pass filter.

Masao et al disclose wherein an inductor comprised of part of said inductor electrodes (7 on bottom green sheet 1a) not to be sandwiched by said plurality of grounded electrodes is used in a filter, and the inductor (3a on layer 1b) comprised of the inductor electrodes other than said part thereof (part sandwiched between layer 1c and 1a) is used in a filter (paras. 9-10). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the inductor electrodes in a filter in order to allow the filter to have high inductance as suggested by Masao et al (para.1).

Toshihiko et al and Masao et al do not disclose the inductor electrodes are used in a band pass filter or a high pass filter. However, it is well known in the art that a filter can be band pass or high pass based on the desired frequency response. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the inductor be used in a band pass or high pass filter based on which unwanted frequencies the electronic component needs to filter out to optimize conductance.

Regarding claim 18, Toshihiko et al disclose the multilayer electronic component according to claim 3, wherein Toshihiko et al do not disclose an inductor comprised of part of said inductor electrodes not to be sandwiched by said plurality of grounded electrodes is used in a low-pass filter, and the inductor comprised of the inductor electrodes other than said part thereof is used in a band-pass filter.

Masao et al disclose wherein an inductor comprised of part of said inductor electrodes (7 on bottom green sheet 1a) not to be sandwiched by said plurality of grounded electrodes is used in an LC filter, and the inductor (3a on layer 1b) comprised of the inductor electrodes other than said part thereof (part sandwiched between layer 1c and 1a) is used in an LC filter (paras. 9-10). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the inductor electrodes in a filter in order to allow the filter to have high inductance as suggested by Masao et al (para.1).

Toshihiko et al and Masao et al do not disclose the inductor electrodes are used in a band pass filter or a low pass filter. However, it is well known in the art that a filter can

be band pass or low pass based on the desired frequency response. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the inductor be used in a band pass or low pass filter based on which unwanted frequencies the electronic component needs to filter out to optimize conductance.

Regarding claim 19, Toshihiko et al disclose the multilayer electronic component according to claim 3, wherein first inductor comprised of part of said inductor electrodes not to be sandwiched by said plurality of grounded electrodes is used in a band pass filter, and inductor comprised of the inductor electrodes other than said part thereof used a band pass filter of a frequency band higher than the band pass filter using the inductor formed by said first inductor electrodes.

Toshihiko et al disclose wherein an inductor comprised of part of said inductor electrodes (7 on bottom green sheet 1a) not to be sandwiched by said plurality of grounded electrodes is used in an LC filter, and the inductor (3a on layer 1b) comprised of the inductor electrodes other than said part thereof (part sandwiched between layer 1c and 1a) is used in an LC filter (paras. 9-10). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the inductor electrodes in a filter in order to allow the filter to have high inductance as suggested by Masao et al (para.1).

Toshihiko et al and Masao et al do not disclose the inductor electrodes are used in different passband band pass filters. However, it is well known in the art that a filter can be band pass at a certain band based on the desired frequencies. Therefore, it would

have been obvious to one of ordinary skill in the art at the time the invention was made to have the inductor be used in a band pass or low pass filter based on which unwanted frequencies the electronic component needs to filter out to optimize conductance.

4. Claims 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toshihiko et al (JP 09-320849) in view of Watanabe et al (US 2004/0,087,280).

Regarding claim 20, Toshihiko et al the multilayer electronic component according to claim 3 wherein Toshihiko et al disclose an inductor comprised of part of said inductor electrodes not to be sandwiched by said plurality of grounded electrodes and inductors electrodes other than said part thereof is used in a digital radiotelephone (para. 2). Toshihiko et al do not explicitly disclose inductors not to be sandwiched by said plurality of grounded electrodes is used in a GSM circuit and the inductor comprised of the inductor electrodes other than said part thereof is used in DCS circuit. However, it is well known in the cellular communications that digital cellular system comprises GSM and DCS as taught by Wantanabe. Wantanabe disclose the inductor electrodes of a high frequency component is formed in the GSM system and DCS system (paras. 106, 140). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the inductor electrode of Toshihiko et al be in a GSM and DCS circuit in order to install the chip containing the inductor electrodes be applicable to the digital phone of Toshihiko et al in a particular digital system based on which system the phone is operating in.

Regarding claim 21, Toshihiko et al the multilayer electronic component according to claim 3 wherein Toshihiko et al disclose an inductor comprised of part of said inductor electrodes not to be sandwiched by said plurality of grounded electrodes and inductors electrodes other than said part thereof is used in an analog or digital radiotelephone (para. 2). Toshihiko et al do not explicitly disclose inductors not to be sandwiched by said plurality of grounded electrodes is used in an AMPS circuit and the inductor comprised of the inductor electrodes other than said part thereof is used in a CDMA2000 circuit. However, it is well known in the cellular communications that cellular systems comprises AMPS and CDMA2000 as taught by Wantanabe. Wantanabe disclose the inductor electrodes of a high frequency component is formed in an analog AMPS system or CDMA2000 system (paras. 106, 140). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the inductor electrode of Toshihiko et al be in a GSM and DCS circuit in order to install the chip containing the inductor electrodes be applicable to the digital phone of Toshihiko et al in a particular system in which the phone is operating in.

Regarding claim 22, Toshihiko et al disclose the multilayer electronic component according to claim 3 wherein Toshihiko et al do not disclose an inductor comprised of part of said inductor electrodes not to be sandwiched by said plurality of grounded electrodes is used in a PDC circuit and the inductor comprised of the inductor electrodes other than said part thereof is used in a W-CDMA circuit. However, it is well known in the cellular communications that digital cellular system comprises PDC and W-CDMA as taught by Wantanabe. Wantanabe disclose the inductor electrodes of a

high frequency component is formed in PDC and W-CDMA systems (paras. 106, 140). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the inductor electrode of Toshihiko et al be in a PDC and a W-CDMA circuit in order to install the chip containing the inductor electrodes be applicable to the digital phone of Toshihiko et al in a particular system based on which system the phone is operating in.

Regarding claim 23, Toshihiko et al the multilayer electronic component according to claim 3 wherein Toshihiko et al disclose an inductor comprised of part of said inductor electrodes not to be sandwiched by said plurality of grounded electrodes and inductors electrodes other than said part thereof is used in a digital radiotelephone (para. 2). Toshihiko et al do not explicitly disclose inductors not to be sandwiched by said plurality of grounded electrodes is used in a GSM circuit and the inductor comprised of the inductor electrodes other than said part thereof is used in a W-CDMA circuit. However, it is well known in the cellular communications that digital cellular system comprises GSM and W-CDMA as taught by Wantanabe. Wantanabe disclose the inductor electrodes of a high frequency component is formed in the GSM system and W-CDMA system (paras. 106, 140). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the inductor electrode of Toshihiko et al be in a GSM and a W-CDMA circuit in order to install the chip containing the inductor electrodes be applicable to the digital phone of Toshihiko et al in a particular digital system based on which system the phone is operating in.

Regarding claim 24, Toshihiko et al the multilayer electronic component according to claim 3 wherein Toshihiko et al disclose an inductor comprised of part of said inductor electrodes not to be sandwiched by said plurality of grounded electrodes and inductors electrodes other than said part thereof is used in a digital radiotelephone (para. 2). Toshihiko et al do not explicitly disclose inductors not to be sandwiched by said plurality of grounded electrodes is used in a DCS circuit and the inductor comprised of the inductor electrodes other than said part thereof is used in W-CDMA circuit. However, it is well known in the cellular communications that digital cellular system comprises DCS and W-CDMA as taught by Wantanabe. Wantanabe disclose the inductor electrodes of a high frequency component is formed in the DCS system and W-CDMA system (paras. 106, 140). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the inductor electrode of Toshihiko et al be in a DCS and W-CDMA circuit in order to install the chip containing the inductor electrodes be applicable to the digital phone of Toshihiko et al in a particular digital system based on which system the phone is operating in.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toshihiko et al (JP 09-320,849) in view of Asakura et al (US 6,002,576).

Regarding claim 4, Toshihiko et al disclose the multilayer electronic component according to claim 1, wherein Toshihiko et al do not disclose all or part of said inductor electrodes not sandwiched by said plurality of grounded electrodes are placed on the dielectric sheets not sandwiched by said plurality of grounded electrodes. Asakura et al disclose all or part of capacitor electrodes (3; fig. 1) not sandwiched by said plurality of grounded electrodes are placed on the dielectric sheets (top surface of top dielectric sheet 2) not sandwiched by said plurality of grounded electrodes (bottom laminate layer 2 of each dielectric sheet). It would have been obvious to one of ordinary skill in the art at the time the invention was made to place the conductive electrodes on a dielectric sheet not sandwiched on by the ground electrodes in order to allow trimming of the conductive electrode to reduce the Q value from the top dielectric sheet as suggested by Asakura et al (col 3, lines 39-49).

Regarding claim 7, Toshihiko et al disclose the multilayer electronic component according to claim 1 or 3, wherein Toshihiko et al do not disclose all or part of said inductor electrodes not sandwiched by said plurality of grounded electrodes by said plurality of grounded electrodes are formed by having slots having substantially the same shape as said inductor electrodes formed on said grounded electrodes overlap said inductor electrodes. Asakura et al disclose all or part of said inductor electrodes not sandwiched by said plurality of grounded electrodes by said plurality of grounded

electrodes are formed by having slots (3, 4, 5) having substantially the same shape as said inductor electrodes formed on said grounded electrodes overlap said inductor electrodes (fig. 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the same shape conductor be on the top layer in order to have the same type of conductor on all the dielectric sheets.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lana N Le whose telephone number is (703) 308-5836. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward F Urban can be reached on (703) 305-4385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lana Le

Lana Le

June 12, 2005